HOET23281:- Advanced Digital System Design

Teaching Scheme: Theory: 02 Hours/Week Practical: 02 Hours/Week	Credits 03	Examination Scheme: Activity:10 Marks In Sem: 20 Marks End Sem:50 Marks Practical: 20 Marks Teamwork: 20 Marks

Prior knowledge of

1. Digital Logic Design

is essential.

Course Objectives:

1. To explore Hardware Description Language (HDL) and respective digital design methodologies.
2. Understand the various abstraction levels in Verilog HDL and thus model tasks & functions at a behavioural level.
3. Model the state machines using D and JK Flip Flops and design the complex combinational and sequential logic circuits using various constructs in Verilog.
4. Understand the types of programmable logic devices and building blocks of FPGA and thus implement the design using Xilinx

Course Outcomes:

1. Write Verilog HDL code and thus model tasks & functions at the behavioural level
2. Design the state machines using D and JK Flip Flops and model using Verilog
3. To model combinational circuits and sequential circuits using Verilog.
4. Differentiate FPGAs and Implement digital design on FPGA

Course Contents

Unit I: Verilog HDL (06 Hrs.)

Data Flow & Structural Modeling-Lexical Conventions - Ports and Modules – Operators - Gate Level Modeling - Data Flow Modeling - System Tasks & Compiler Directives - Test Bench. Behavioural level Modeling- Procedural Assignment Statements- Blocking and Non-Blocking Assignments -Tasks & Functions - Useful Modeling Techniques.

Unit II: State Machine Design (06 Hrs.)

Definition of state machines -State machine as a sequential controller- Analysis of state machines using D and JK flip-flops - Design of state machines- State table and State assignment - Transition/excitation table - excitation maps and equations - logic realization- Design examples, State Minimization Techniques, State partition method.

Unit III: Combinational Circuits and Verilog Modelling (06 Hrs.)

Adders: Ripple Carry Adder, Carry Look-Ahead Adder, Higher Bit Adders Using CLA, Manchester Carry Chain Module (MCC), Carry Skip Adder, Carry Increment Adder, Carry Select Adder, Carry Save Addition, BCD Addition. Multipliers: Sequential Multiplication, Array Multipliers, Partial

Product Generation and Reduction, Booth's Multiplication, Multiplication Using Look-Up Table

Unit IV: Sequential Circuits and Verilog Modelling (06 Hrs.)

Sequential Circuits: BCD up-down counter, Synchronous and Asynchronous FIFO – Single port and Dual port ROM and RAM - FSM Verilog modelling of Sequence detector - Serial adder - Vending machine. Design Guidelines for Sequential Circuits

Unit V: Complex Operations and Algorithms (06 Hrs.)

Sequential Division method, Fast division algorithms, Iterative division algorithms, Computation of modulus, Square root and reciprocal, Tailor series expansion, CORDIC algorithm and applications, VEDIC Architectures.

Unit VI: FPGA Architecture and Design Flow (06 Hrs.)

Types of Programmable Logic Devices: PLA, PAL, CPLD - FPGA Architecture - Programming Technologies-Chip I/O- Programmable Logic Blocks- Fabric and Architecture of FPGA. Impacts of logic block functionality on FPGA performance, Model for measuring delay.

FPGA Families: Artix, Kintex, Virtex, EDA tools, Design Flow, FPGA Design Guidelines.

Text Books:

T1. Samir Palnitkar, "Verilog HDL", 2nd Edition, Pearson Education.

T2. Advanced Digital System Design A Practical Guide to Verilog-based FPGA and ASIC Implementation.

Reference Books:

R1. Data sheets of Artix-7, Kintex-7, Virtex-7.

R2. Digital Logic Design Using Verilog, Coding and RTL Synthesis by Vaibhav Taraate, Second Edition Springer

R3. Advanced Digital Logic Design using Verilog, State Machines & Synthesis for FPGA - Sunggu Lee, Cengage Learning.

NPTEL:

1. Digital Design with Verilog By Prof. Chandan Karfa, Prof. Aryabartta Sahu, IIT Guwahati https://onlinecourses.nptel.ac.in/noc24_cs61/preview

2. System Design Through VERILOG By Prof. Shaik Rafi Ahamed, IIT Guwahati https://onlinecourses.nptel.ac.in/noc21_ee97/preview

List of Experiments

1. Introduction to FPGA design flow using Verilog
2. Design and implementation of Adder and compare the performance with other adder circuits.
3. Design and implement a multiplier and compare its performance with that of other multiplier circuits.
4. Design and implement BCD up-down counter
5. Design and implement FIFO

6. Design and implement Serial adder/Sequence Detector/Vending Machine

7. Mini Project: Design and implement Microcontroller OR Communication Protocol or any equivalent design on BASYS 3 Kit. A group of 4-5 students will design the individual modules of the project and integrate the complete design.

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